[0079] **CLAIMS**

[0080] We claim:

1. A method of preparing a sample of a semiconductor structure for adhesion testing, comprising:

a) providing a first semiconductor structure comprising at least one layer of additive material overlying a first crystalline semiconductor substrate, wherein said at least one layer of additive material is different from said crystalline substrate;

b) providing a second semiconductor structure comprising a second crystalline semiconductor substrate, wherein said second semiconductor substrate is the same material as said first semiconductor substrate;

c) providing an adhesive on an exposed surface of said at least one layer of additive material;

d) aligning said first semiconductor structure and said second semiconductor structure crystalline lattice structures, with an exposed surface of said at least one layer of additive material in contact with an exposed surface of said second semiconductor structure, with a layer of said adhesive between said additive material layer and said second semiconductor structure;

e) curing said adhesive, to bond said exposed surface of said at least one layer of additive material to said exposed surface of said second semiconductor structure, whereby a bonded sandwich structure is formed;

f) making at least one scribe extending across an edge portion of an exposed upper surface of said first crystalline semiconductor substrate, and downward across an exposed side surface of said first crystalline semiconductor substrate, an exposed side surface of said at

least one layer of additive material, and at least a portion of an exposed side surface of said second crystalline semiconductor substrate; and

g) breaking said bonded sandwich structure along a crystalline lattice structure direction to form at least one test specimen.

2. The method of Claim 1, including an additional step following step g), said additional step comprising:

h) making a scribe on an exposed major crystalline substrate surface of said test specimen, wherein said scribe extends in a straight line across a width of said test specimen, in a direction perpendicular to a crystalline lattice structure direction, from a first long edge of said test specimen to an opposing long edge of said test specimen, and wherein said scribe crosses a corner of said first long edge and a corner of said second long edge.

3. The method of Claim 1 or Claim 2, wherein said crystalline substrate is selected from the group consisting of single-crystal silicon and gallium arsenide.

4. The method of Claim 1 or Claim 2, wherein said at least one layer of additive material was deposited using a deposition technique selected from the group consisting of chemical vapor deposition, physical vapor deposition, and spin-on.

5. The method of Claim 1 or Claim 2, wherein said at least one layer of additive material has a thickness of 10 microns or less.

6. The method of Claim 1 or Claim 2, wherein said at least one layer of additive material is selected from the group consisting of a metal, a metal nitride, a metal oxide, a silicon-containing material, and an organic material.

7. The method of Claim 6, wherein said at least one layer of additive material is a metal selected from the group consisting of aluminum, copper, platinum, iridium, ruthenium, titanium, tantalum, and tungsten.

8. The method of Claim 6, wherein said at least one layer of additive material is a metal nitride selected from the group consisting of titanium nitride, tantalum nitride, and tungsten nitride.

9. The method of Claim 6, wherein said at least one layer of additive material is a metal oxide selected from the group consisting of aluminum oxide, iridium oxide, and ruthenium oxide.

10. The method of Claim 6, wherein said at least one layer of additive material is a silicon-containing material selected from the group consisting of polysilicon, silicon oxide, silicon nitride, silicon oxynitride, and silicon carbide.

11. The method of Claim 1 or Claim 2, wherein said second semiconductor structure has the same structure as said first semiconductor structure, wherein said first semiconductor structure and said second semiconductor structure are aligned so that an exposed surface of said at least one layer of additive material of said first semiconductor structure is in contact with an exposed surface of at least one layer of additive material of said second semiconductor structure,

with a layer of said adhesive between said additive material layer of said first semiconductor structure and said additive material layer of said second semiconductor structure.

12. The method of Claim 1 or Claim 2, wherein said adhesive is an epoxy adhesive.

13. The method of Claim 1 or Claim 2, wherein said adhesive layer has a thickness within the range of about 2 μm to about 20 μm.

14. The method of Claim 1 or Claim 2, wherein said crystalline substrate comprises single-crystal silicon, and wherein said first scribe and said second scribe are perpendicular to a silicon <100> crystal orientation.

15. The method of Claim 2, wherein said step h) scribe is formed to a depth which is about 0.3 % to about 10 % of the thickness of a crystalline layer of substrate which is scribed.

16. The method of Claim 2, wherein said step h) scribe on said exposed major crystalline substrate surface of said test specimen, extends over each said corner of said long edge for a distance down a sidewall of said test specimen of about 1.3 % to about 50 % of the thickness of a crystalline layer which provides said exposed major substrate surface.

17. The method of Claim 16, wherein said step h) scribe on said exposed major crystalline substrate surface of said test specimen, extends over each said corner of said long edge for a distance down a sidewall of said test specimen of about 1.3 % to about 10 % of the thickness of a crystalline layer which provides said exposed major substrate surface.

18. A test specimen preparation fixture for preparing a test specimen of a semiconductor structure for adhesion testing, wherein said test specimen preparation fixture comprises:

a) a base having an upward-facing wedge structure over a portion of an upper surface of said base; and

b) a cover having downward-facing structures adapted for gripping an upper surface of a test specimen, wherein said downward-facing structures are positioned along an area of said cover which faces said upward-facing wedge structure on said base.

19. The test specimen preparation fixture of Claim 18, wherein said base has a width ranging from about 30 mm to about 40 mm, and a length ranging from about 30 mm to about 40 mm.

20. The test specimen preparation fixture of Claim 18, wherein said cover has width ranging from about 10 mm to about 40 mm, and a length ranging from about 30 mm to about 40 mm.

21. The test specimen preparation fixture of Claim 18, wherein said wedge has a height ranging from about 1 mm to about 2 mm, a width of about 2 mm, and a length ranging from about 3 mm to about 4 mm.

22. The test specimen preparation fixture of Claim 21, wherein said wedge has an upper edge radius of 0.5 mm or less.

23. The test specimen preparation fixture of Claim 18, wherein said structures adapted for gripping said bonded sandwich structure have a height ranging from about 2 mm to about 5 mm.

24. The test specimen preparation fixture of Claim 18, wherein said structures adapted for gripping are at least two structures, and wherein said structures for gripping are spaced apart across the width of said fixture so that gripping structures nearest the lengthwise centerline of said fixture are positioned at least about 5 mm away from said lengthwise centerline of said fixture.

25. A method of preparing a test specimen using the test specimen preparation fixture of Claim 18, wherein said method comprises the steps of:

a) providing a bonded sandwich structure comprising a first semiconductor structure adhesively bonded to a second semiconductor structure, wherein each major exterior surface of said bonded sandwich structure is a crystalline material having an essentially continuous crystal lattice structure, wherein said crystal lattice structure of each major exterior surface is aligned to be parallel, and wherein said bonded sandwich structure includes a scribe in alignment with a direction of said crystal lattice;

b) positioning said bonded sandwich structure upon said base of said test specimen preparation fixture such that a centerline of said scribe is aligned with a centerline of a wedge structure present on said base;

c) placing said cover of said test specimen preparation fixture on top of said bonded sandwich structure, such that said structures adapted for gripping said bonded sandwich structure contact a top surface of said bonded sandwich structure; and

d) applying uniform pressure along all four corners of said cover of said test specimen preparation fixture, whereby said wedge, operating in combination with said scribe, initiates and propagates a break along a crystalline boundary of said bonded sandwich structure.

26. The method of Claim 25, wherein said second semiconductor structure has the same crystalline lattice structure as said first semiconductor structure.